REMARKS

The specification has been amended to address typographical errors and inconsistencies noted by the Examiner as discussed in further detail hereinbelow. Claims 1, 2, 6, 7, 8, 9, 10 and 18 have been amended to more particularly point out the novelty of the embodiments of the present invention. Applicants believe no new matter has been added.

FIG. 3 has been corrected to renumber the reference numeral for the demodulation box to be 88 which corresponds to the reference numeral in the specification. A substitute FIG. 3 is provided.

The use of the trademark FireWire® has been amended to include generic terminology of the use of a high speed serial data bus. Applicants acknowledge with thanks for the Examiner noting the use of the trademark FireWire®.

The specification has been amended to include descriptions for the reference numerals 52, 78, 154, 192 and 194.

Claims 2, 10 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention.

Claims 2, 10 and 18 have been amended to more particularly point out and distinctly claim the subject matter. In particular the term "high-resolution" has been replaced in claims 2 and 10. Claim 18 has been amended to recite the use of a high speed data bus interface as opposed to the use of the trademark FireWire®.

Claim Amendments Under 37 C.F.R. § 1.102(b)

Claims 1, 6-9 and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kosalos et al.

Claims 1, 2, 6-10 and 18 have been amended to more particularly point out and distinctly claim the subject matter. In particular, the amended claims recite the use of beamforming devices each device being formed on a single integrated circuit. The

Kosalos et al. reference does not disclose the use of a beamforming device formed on a single integrated circuit.

Claim Amendments Under 37 C.F.R. § 1.103(a)

Claims 2, 10, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosalos et al. in combination with Kits van Heyningen.

Claims 1, 2, 6-10 and 18 have been amended to more particularly point out and distinctly claim the subject matter. In particular, the amended claims recite the use of beamforming devices formed on a single integrated circuit. The Kosalos et al. reference does not disclose the use of a beamforming device formed on a single integrated circuit. The Kits van Heyningen reference also does not teach or suggest the use of a beamformer formed on a single integrated circuit.

Claim Amendments Under 37 C.F.R. § 1.103(a)

Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosalos et al. in combination with Gilmour.

Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosalos et al. in combination with Morgera.

Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosalos et al. in combination with English.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kosalos et al. in combination with Gilbert et al.

Claim 20 is rejected under 35 U.S.C. 103 as being unpatentable over Kosalos et al. in combination with Kits van Heyningen as applied to claim 19 above, and further in combination with Gerard.

Claims 1, 2, 6-10 and 18 have been amended to more particularly point out and distinctly claim the subject matter. In particular, the amended claims recite the use of beamforming devices formed on a single integrated circuit. The Kosalos et al. reference does not disclose the use of a beamforming device formed on a single integrated circuit. The combination of Gilmour, Morgera, English, Kits van Heyningen and Gerard,

respectively, in combination with Kosalos et al. do not teach or suggest the teachings of the amended claims.

CONCLUSION

In view of the amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone call would expedite the prosecution of this case, the Examiner is invited to call the undersigned at (508) 879-5700.

Respectfully submitted,

BOWDITCH & DEWEY, LLP

By _____

Thomas O. Hoover
Registration No.: 32,470
Telephone: (508) 879-5700
Facsimile: (508) 929-3073

Framingham, Massachusetts 01701-9320
Dated: March 24, 2003

MARKED UP VERSION OF AMENDMENTS

Specification Amendments Under 37 C.F. R. § 1.121(b)(1)(iii)

Please replace the paragraph starting at page 11, line 17 and ending on page 12, line 2 with the following paragraph:

Figure 2 is a diagram illustrating another preferred embodiment of a sonar beamforming system 40 in accordance with the present invention. This system 40 includes a forward-looking sonar 44 having forward-looking sonar transmit beams 48 and forward-looking sonar receive beams 50. In addition, the system 40 has two side scan sonars 46 having side-looking sonar transmit beams 52. Further acoustic communication devices 54 which are preferably steerable are also present in this preferred embodiment of the system. At least one identification sonar 60 or a downward-looking Bathymetric Sonar is also mounted on the underside of the vehicle that transmits beam 58 and receives beams 56. This Bathymetric sonar 60 is a downward-looking sonar (DLS) for high-resolution terrain mapping and object identification.

Please replace the paragraph starting at page 12, line 16 and ending on page 13, line 6 with the following paragraph:

Figure 3 is a block diagram illustrating an electronic focusing sonar imaging system 70 in accordance with a preferred embodiment of the present invention. Signals such as transducer signal 74 and output signals 76 form the input to a low noise preamplifier 72 having time-gain control. The output of the preamplifier 72 forms the input into a sampling subsystem 80. The output of the sampler forms the input to programmable delays 82 associated with beamsteering and focusing functions, the output of which forms an input into a weighting subsystem 84. The outputs of the weighting function are then summed in a summer 86. In a preferred embodiment the sampler 80, the programmable delays 82, the weighting function 84 and summer 86 functions are integrated on a single chip 78 which accomplishes beamforming, preferably using a charge-domain-processing (CDP) structure. A preferred implementation of a beamforming device using CDP technology, including a programmable tapped delay line structure, is described in a co-pending PCT International Application Number

PCT/US98/02291, filed on 3 February 1998, by Jeffrey Gilbert, Alice Chiang, and Steven Broadstone, the entire contents of which is hereby incorporated by reference.

Please replace the paragraph on page 14, lines 3 through 22 with the following paragraph:

The front-end 102 of the system 100 is an integration of many subsystems. A waveform transmit function 112 forms an input to a transmitter 114 which in turn transmits waveforms to a target image 106. An array 116 is received at the front-end 102 from the target image and is then processed in the front-end. The array in a preferred embodiment is a one-dimensional array. The processing signals of the received array begins with preamplification in a low noise preamplifier 118 having time-gain control. The output of the preamplifier 118 forms the input into a beamforming function 124, preferably using CDP. A memory device 122 interfaces with the preamplifier 118 and the beamformer 124. The memory device 122 may be a single memory device or plurality of memory devices. Such a memory device may be, but is not limited to, a random access memory, read-only memory, floppy disk memory, hard drive memory, extended memory, magnetic tape memory, zip drive memory and/or any device that stores digital information. A front-end host interface processing module or controller 120 interfaces with the memory 122. The controller 120 may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcomputer, digital signal processor, central processing unit of a computer or work station, digital circuitry, state machine, and/or any device that manipulates signals, for example, analog and/or digital, based on operational instructions. It should be noted that when the processing module implements one or more functions, via a state machine or logic circuitry, the memory storing the corresponding operational instructions is embedded within the circuitry comprising the state machine or logic circuitry. A standard interface such as, for example, a high-speed serial bus [IEEE 1394/Firewire] IEEE 1394/FireWire® chip set 126 interfaces with both the host interface controller 120 and the memory 122.

Please replace the paragraph on page 15, lines 9 through 16 with the following paragraph:

The back-end 104 includes a microprocessor 130 that sends inputs to an Interface chip [(IEEE1394)] (IEEE 1394) 134 and then to a buffer 128 and a post signal processor 132. The [Firewire] FireWire® (IEEE 1394) chip set 126 in the front-end 102 interfaces with the interface chip set 134 in the back-end through an interface 110. The back-end preferably includes a receiving [parellel] parallel data bus interface, for example, PCI or a serial bus interface, for example, a [Firewire] FireWire® chip set 134. The buffer 128 interfaces with the post signal processor 132. Further details regarding interface structure can be found in U.S. Application No. 09/791,491 filed on February 22, 2001, the entire contents of which is incorporated herein by reference.

Please replace the paragraph starting at page 15, line 21 and ending on page 16, line 8 with the following paragraph:

Figure 5 is a block diagram illustrating a flow chart of the image fusion process 150 of the sonar imaging system in accordance with a preferred embodiment of the present invention. Data from at least one side scan 152 are meshed with forward scan 152, 154 data 156 derived from a forward-looking scan such as described with respect to Figures 1 and 2. This data from the side scan and the forward scan are first normalized or scaled in a normalizing process 158. The process of normalization addresses spatial resolution. This normalization process is preferably performed, without limitation, on a standard personal computer platform. The fan shaped data is then meshed in an image fusion process 160. The data fusion process enables multi-sensor target classification and identification. The data fusion process may be accomplished, without limitation, using commercial products which provide three-dimensional rendering of data that is stacked such as, for example, 3D EchoTech that is provided commercially by EchoTech.

Please replace the paragraph on page 16, lines 13 through 15 with the following paragraph:

Figure 7 is a graphical illustration 190 of a curvilinear array of a sonar imaging system in accordance with a preferred embodiment of the present invention. An ultrasound absorbent backing layer 192 is used to generate a transducer frequency

response with a wide bandwidth. The curvilinear array has a plurality of ultrasound elements 194. The FLS curvilinear receive array has a center frequency between 500 Hz to 1 MHz with 192 elements.

Claim Amendments Under 37 C.F.R. § 1.112

1. (Amended) A sonar beamforming system, comprising in combination:

a forward-looking sonar having transmit and receive transducer arrays and a programmable beamforming device formed on a single integrated circuit; and

at least one side-looking sonar having multi-element arrays and a second beamforming device formed on a second single integrated circuit.

2. (Amended) The system of claim 1, further comprising a downward-looking sonar [for high-resolution] having sufficient resolution for terrain mapping and object identification.

6. (Amended) A water craft, comprising in combination at least one of:

a forward-looking sonar having a transmit and receive transducer array and a programmable beamforming device formed on a single integrated circuit; and

a side-looking sonar having multi-element arrays and a beamforming device formed on a second single integrated circuit.

7. (Amended) A forward-looking sonar comprising in combination:

a bistatic transducer array having a first transmit transducer array and a second receive transducer array;

a beamforming device formed on a single integrated circuit; and

a processing unit.

8. (Amended) A method for forming an integrated image comprising the steps of:

obtaining array signals from a forward-looking sonar having a programmable beamformer circuit formed on a single integrated circuit;

obtaining array signals from at least one side-looking sonar;

normalizing the array signals from the forward-looking sonar and the at least one side-looking sonar to generate normalized data using a personal computer platform; and

fusing the normalized data to generate an image.

9. (Amended) An underwater unmanned vehicle system comprising in combination:

a forward-looking sonar having a transmit and receive transducer array and a beamforming device formed on a single integrated circuit; and

at least one side-looking sonar having a second transducer array and a beamforming device formed on a second integrated circuit.

10. (Amended) The system of claim 9, further comprising a downward-looking sonar [for high-resolution] having sufficient resolution for terrain mapping and object identification.

18. (Amended) The system of claim 17, further comprising a [Firewire] high speed data bus interface connected to the interface controller and the memory circuit, the [Firewire] high speed data bus interface communicating with the central processor.